LEARNING MODULE DESCRIPTION

GENERAL INFORMATION

1. Module title: Design of logic circuits
2. USOS code: 04-W-LIS-45
3. Term: winter
4. Duration: 15L + 30Classes
5. ECTS: 5
6. Module lecturer: Michał Tanaś
7. E-mail: mtanas@amu.edu.pl
8. Language: english

DETAILED INFORMATION

1. Module aim (aims)

The module aims to teach students the general rules of design of logic circuits as well as how to design the main classes of logic circuits which are: combinatorial circuits (multiplexers and demultiplexers), arithmetic circuits (adders and subtractors) and memory circuits (static RAM). The secondary objective of this module is to teach students foundations of VHDL hardware design language and basics of testing of logic circuits (testbenches).

2. Pre-requisites in terms of knowledge, skills and social competences (where relevant)

- Basic computer related skills – e.g. skill in using web browsers, installing software, using e-mails, etc.
- English language knowledge enough to read technical documentation and using software in English language
- Basic knowledge about mathematical logic (Boolean expressions)

READING LIST

H.Roth, L.K. John, „Digital Systems Design Using VHDL", CL ENGINEERING, ISBN: 978-13-056-3514-2

SYLLABUS:

Week 1: Boolean logic and digital signals waveforms
Week 2: Introduction to Xilinx ISE
Week 3: Introduction to VHDL
Week 4: Testbenches and ISIM simulator
Week 5: Schematics diagrams
Week 6: Basic logic gates and tables of truth
Week 7: Combination of logic gates
Week 8: 2-inputs multiplexers
Week 9: 2-inputs demultiplexers
Week 10: multiinputs multiplexers and demultiplexers
Week 11: half-adders
Week 12: combination of half adders and carry signal
Week 13: subtractors
Week 14: flip-flops
Week 15: static RAM circuits